REMARKS

Claims 2-23 are pending and unamended. Claim 1 was previously canceled and not withdrawn from consideration as listed on the Office Action Summary. Withdrawal of all claim rejections is respectfully requested for at least the reasons set forth below.

Prior Art Rejection

Claims 2-23 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Nos. 6,746,893 and 6,794,255 (Forbes et al.), hereinafter, "Forbes '893" and "Forbes '255," respectively. Applicants respectfully request withdrawal of the rejection for at least the reasons set forth below.

1. Patentability of independent claims 11 and 19 over Forbes '893

The Examiner asserts that Forbes '893 discloses all of the features of claims 11 and 19 of the present application. This is incorrect. Claim 11 recites, in part, "the floating gate comprises a microcrystalline material having a grain size of about 50Å – 300Å." Claim 19 recites, in part, "the floating gate comprises one of amorphous silicon or polysilicon having a grain size of 50Å – 300Å." Forbes does not disclose that the floating gate has a grain size of 50Å – 300Å. The Examiner asserts that Forbes '893 discloses the floating gate grain size in column 6, lines 26-37, which reads as follows:

> The upper layers, such as layer 112 are covered with a layer 116 of a suitable insulating material in the conventional manner, such as for isolating and protecting the physical integrity of the underlying features. Gate 106 is isolated from channel 110 by an insulating layer such as thin oxide layer 118, or any other suitable dielectric material. In one embodiment, thin oxide layer 118 is a gate oxide layer that can be approximately 100 angstroms (Å) thick, such as for conventional FET operation. In another embodiment, such as in a floating gate transistor, thin oxide layer 118 is a tunnel oxide material that can be approximately 50-100 Å thick. (Underlining added for emphasis)

The above paragraph of Forbes '893 discloses that the grain size of the thin oxide insulating layer 118 can be approximately 50Å – 100Å thick. The thin oxide layer 118 is not the same, or equivalent to, the claimed "floating gate." Instead, it is an insulating layer that isolates the floating gate 106 from the channel 110. The thickness of the thin oxide layer 118 does not disclose or suggest any particular grain size for the floating gate 106.

In summary, Forbes '893 does not disclose or suggest any grain size for the floating gate. In view of the above, the rejection of claims 11 and 19 should be withdrawn.

2. Patentability of independent claim 13 over Forbes '255

The Examiner asserts that Forbes discloses all of the features of claim 13 of the present application. Claim 13 recites, in part, "thermally treating the memory cell to transform the amorphous material [of the floating gate] into a microcrystalline material." The "thermally treating" step is described on page 7, lines 16-22 of the present application, which reads as follows:

> [021] In another aspect, the step of forming floating gate 112 comprises forming a layer of amorphous silicon over first insulating layer 110. A step of thermal treatment follows to transform the amorphous silicon into polysilicon with a grain size of about 200-500 Å. In one aspect, the thermal treatment is performed in a conventional vertical furnace or rapid thermal process apparatus, with reaction gases including N_2, O_2, H_2, N_2O. In another aspect, the thermal treatment is performed at a temperature of about 800°C - 1000°C (underlining for emphasis)

As disclosed in the above paragraph, the floating gate is an amorphous material that undergoes a step of thermal treatment to transform the amorphous material into a microcrystalline material. The Examiner states that Forbes '255 discloses the thermal treatment in column 4, lines 4-46, which reads as follows:

> In one embodiment, the SiC layer 118 is grown in a microwave-plasma-enhanced chemical vapor deposition (MPECVD) system. A silicon substrate is first etched in dilute HF for about one minute and thoroughly rinsed in deionized water prior to insertion into a reactor, such as an Applied Materials single wafer system, model number 5000, which has

four to five process chambers, each holding one wafer. Following insertion in the chamber, the chamber is first evacuated to a pressure of 10^{-4} or 10^{-5} mTorr. Carburization of silicon is then performed in a 2% to about 10% concentration of CH_4 /H_2 with a chamber pressure of approximately 25 to 15 Torr depending upon the reactor configuration, horizontal or vertical. Typical microwave power is 1,000 watts for an 8 to 10 inch wafer to 250 to 300 watts for 3 to 4 inch wafers. The substrate is immersed roughly 0.5 cm into a resulting plasma The temperature when the wafer is inserted into the reactor is typically about 400 to 500 degrees C., and is quickly ramped up to about 915 to 1250 degrees C. to carburize the silicon. The higher the temperature and concentration of methane in hydrogen, the faster the film growth. In further embodiments, an electrical bias of between zero and 200 volts may be applied during the carburization...

Layers of SiC grown in the above manner are highly amorphous. The risk of obtaining undesired microcrystaline inclusions is gray [sic][1] reduced. In addition, much lower surface state densities are obtained over deposition techniques, resulting in improved FET performance.

In one example, at 915 degrees C. with a 2% concentration of CH_4 /H_2, a 2 nm film of SiC may be grown in about three minutes.

In a second example, at 1250 degrees C. with 4% concentration of CH_4 /H_2, a 4500 Angstrom thickness film can be grown in about one hour. (underlining for emphasis)

This is not a disclosure of thermally treating a memory cell to transform "amorphous material into a microcrystalline material," in which a floating gate comprises the amorphous material that is thermally treated and transformed into a microcrystalline material, as explicitly recited in claim 13. Instead, the thermal treatment disclosed in Forbes '255 is applied to the SiC layer 118, which is an insulating layer below the floating gate 106 and above the channel 110.

Furthermore, Forbes '255 discloses that the insulating layers 118 of SiC grown as described above are highly amorphous and thus Forbes '255 teaches away from transforming amorphous material into a microcrystalline material. That is, Forbes '255 discloses that the

[1] obvious misspelling of "greatly" in Forbes '255

resultant material is highly amorphous, which is opposite from having a resultant microcrystalline material.

In summary, Forbes '255 does not disclose or suggest the thermal treatment limitation in claim 13 and the floating gate transformation of "amorphous material into a microcrystalline material" limitation recited in claim 13. In view of the above, the rejection of claim 13 should be withdrawn.

3. Patentability of dependent claims

The dependent claims are believed to be patentable over Forbes '893 and Forbes '255, because they depend from allowable independent claims and because they recite additional patentable features.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the instant application including claims 2-23 is in condition for allowance. A Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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